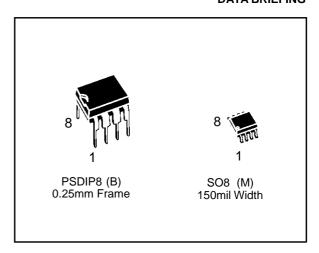


# SERIAL ACCESS SPI BUS 8K (1K x 8) EEPROM

### **DATA BRIEFING**

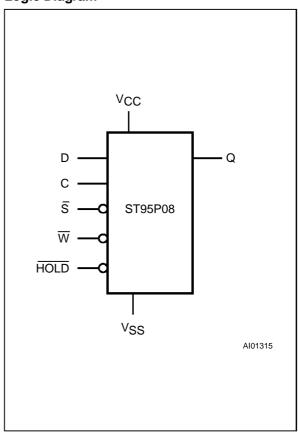
- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE 3V to 5.5V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 2 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- The ST95P08 will be replaced shortly by the updated version ST95080



#### **DESCRIPTION**

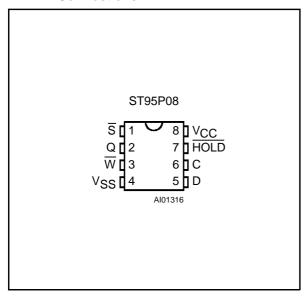
The ST95P08 is a 8K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The 8K bit memory is organised as 64 pages of 16 bytes. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q). The device connected to the bus is selected when the chip select input  $(\overline{S})$  goes low. Communications with the chip can be interrupted with a hold input  $(\overline{HOLD})$ . The write operation is disabled by a write protect input  $(\overline{W})$ .

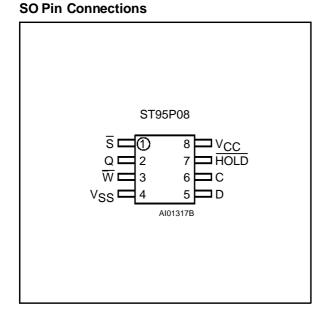
### **Logic Diagram**



B95P08/606 1/2

### **DIP Pin Connections**



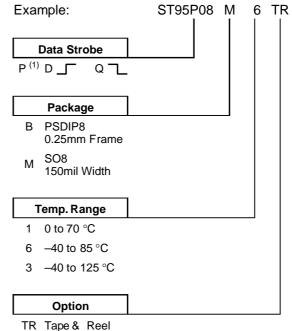


## **Signal Names**

С	Serial Clock
D	Serial Data Input
Q	Serial Data Output
s	Chip Select
W	Write Protect
HOLD	Hold
Vcc	Supply Voltage
V <sub>SS</sub>	Ground

**Ordering Information Scheme**For a list of available options refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.



Note: 1. Data In strobed on rising edge of the clock (C) and Data Out synchronized from the falling edge of the clock.

Packing